



[Handwritten signature]

Docket No.: GR 99 P 1679

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: *Honghong Chen* Date: January 24, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No. : 10/033,227 Confirmation No.: 8514
Inventor : Gerald Deboy, et al.
Filed : October 22, 2001
Title : Semiconductor Component
TC/A.U. : 2822
Examiner : Kiesha L. Rose
Customer No. : 24131

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated August 25, 2004, finally rejecting claims 1-4 and 6-19.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of \$500.00 to cover the fee for filing the *Brief on Appeal*.

02/01/2005 ANAB11 00000076 10033227

01 FC:1402

500.00 OP

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-4 and 6-19 are rejected and are under appeal. Claim 5 has been cancelled. Claims 20-35 have been withdrawn.

Status of Amendments:

No claims were amended after the final Office action. A *Response under 37 CFR § 1.116* was filed on October 29, 2004. The Primary Examiner stated in an *Advisory Action* dated November 22, 2004, that the request for reconsideration had been considered but did not place the application in condition for allowance.

Summary of the Claimed Subject Matter:

The subject matter of claims 1-4 and 6-19 of the instant application is a vertical semiconductor component with a

semiconductor substrate 1 of a first conductivity type (n), a first side I of which is covered by an insulating layer 8 and a second side II of which terminates at a more highly doped layer 2 of the first conductivity type (n+) (see Fig. 2 and page 21, lines 1-10 of the specification). MOS cells (M, SU) are formed in the semiconductor substrate 1 in the region of the first side I, each of which has a well 4, 4' of a second conductivity type (p), a source zone 5, 5' of the first conductivity type (n) embedded in the well, and a source contact 6, 6' contacting the source zone 5, 5' (see Fig. 2 and page 21, lines 12-18 of the specification). The source contact reaches the source zone 5, 5' through the insulating layer 8 (see Fig. 2 and page 21, lines 20-24 of the specification). The MOS cells M, SU further have gate-electrodes 7, 7', which are disposed on a side of the insulating layer 8 remote from the substrate 1 (see Fig. 2 and page 21, line 24 and page 22, line 15 of the specification). The MOS cells are divided into two groups (see Fig. 2 and page 22, lines 3-5 of the specification). The source contacts 6 of the first group M of the MOS cells are electrically insulated from the source contacts 6' of the second group SU of the MOS cells (see Fig. 2 and page 22, lines 12-13 of the specification).

The component according to the invention of the instant application further includes a semiconductor zone 11 of the second conductivity type (p) that is disposed in the semiconductor substrate 1, which reaches to the first side I and is electrically connected with the gate electrode 7' of the second group SU of the MOS cells (see Fig. 2 and page 22, lines 16-22 and page 23, lines 2-4 of the specification).

References Cited:

US 5,296,725	Nandakumar, et al.	March 22, 1994
US 5,780,895	Barret, et al.	July 14, 1998
US 6,359,309 B1	Liao, et al.	March 19, 2002

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 1-4, 7-9, and 11-19 are obvious over Barret et al. in view of Nandakumar et al. under 35 U.S.C. §103.
2. Whether or not claims 6 and 10 are obvious over Barret et al., Nandakumar et al., and further in view of Liao et al. under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2-4 and 6-19 depend on claim 1. The patentability of claims 2-4 and 6-19 are not separately argued. Therefore, claims 2-4 and 6-19 stand or fall with claim 1.

Arguments:

In the section entitled "Claim Rejections - 35 USC § 103" on pages 2-4 of the final Office action, claims 1-4, 7-9, and 11-19 have been rejected as being unpatentable over Barret et al. in view of Nandakumar et al. under 35 U.S.C. § 103(a); claims 6 and 10 have been rejected as being unpatentable over Barret et al., Nandakumar et al. and further in view of Liao et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

a region of the second conductivity type being incorporated into said substrate, reaching to said first side, and electrically connecting to said second gate of said further MOS cells, said region having a potential floating relative to the potential of the first and second source regions of said MOS cells and further MOS cells.

An important aspect of a vertical semiconductor component according to claim 1 of the instant application is that there is a semiconductor zone of a second conductivity type in a substrate of a first conductivity type, which is connected to a gate connection of a transistor cell. As can be seen in Fig. 2 of the instant application, which shows a cross-section of a vertical semiconductor, a semiconductor zone (11, 11') of a second conductivity type (p-doped) is disposed in a substrate (1) of a first conductivity type (n-doped) and the semiconductor zone (11, 11') of the second conductivity type is electrically connected to gate connections (7') of a transistor cell (SU).

Neither Barret et al. nor Nandakumar et al. disclose such a device with a semiconductor zone doped complementarily to a semiconductor substrate and connected to a gate electrode of a transistor cell.

Barret et al. describe a vertical semiconductor component with a semiconductor substrate 0 of a first conductivity type, on one side of which a more highly doped semiconductor layer 11 of the first conductivity type is attached (see Fig 3). First MOS cells are disposed in the region of the side of the semiconductor substrate 0 remote from the more highly doped layer 11, each of which has a well 5 of a second conductivity

type, a source zone 2 of the first conductivity type embedded in the well 5, a source contact 3, and a gate electrode 6.

Fig. 3 of Barret et al. shows a further MOS cell with a well 45 of the second conductivity type, in which a source zone 42 of the first conductivity type is embedded. This source zone 42 is contacted through a source electrode 43. All MOS cells in Barret et al. have a common gate electrode 6.

In contrast to the semiconductor component according to claim 1 of the instant application, the component of Barret et al. does not have a semiconductor zone of the second conductivity type in the semiconductor substrate, which contacts the gate electrode 6. This kind of semiconductor zone disposed in the semiconductor substrate and contacting the gate electrode is also not disclosed in Nandakumar et al.

Nandakumar et al. describe a semiconductor component with a semiconductor substrate 16 of a first conductivity type, in which MOS cells are disposed (see Fig. 3). A semiconductor zone 33 of a second conductivity type, which has a terminal contact 55, is disposed in the semiconductor substrate 16. In contrast to the semiconductor component according to claim 1 of the instant application, the terminal contact 55 is not connected to the gate electrodes 38, 46, 54 of the MOS cells. These gate electrodes 38, 46, 54 are jointly connected to a

gate potential V_{GATE} . In contrast, the terminal 55 of the semiconductor zone 33 of the second conductivity type is connected to a cathode of the component (see column 8, lines 46-47 of Nandakumar et al.).

Contrary to the opinion of the Examiner, a combination of the components of Barret et al. and Nandakumar et al. would not lead to a semiconductor component according to claim 1 of the instant application. It is noted that Barret et al. describe a vertical MOS transistor, whereas Nandakumar et al. describe a vertical thyristor, which distinguishes itself by the fact that a semiconductor layer 14 doped complementarily to the semiconductor substrate 16 is applied on the semiconductor substrate 16 in the region of the backside of the component. Since the components of the cited references describe completely different functional principles, a person skilled in the art would not combine Barret et al. and Nandakumar et al. with each other.

The Examiner has stated in the section entitled "Response to Arguments" on page 4 of the final Office action that Fig. 3 of Nandakumar et al. shows a component in which a semiconductor zone of a second conductivity type, which is disposed in a semiconductor substrate, contacts a gate electrode.

Applicants disagree with the Examiner's opinion for the following reasons.

Fig. 3 of Nandakumar et al. discloses a semiconductor component with a semiconductor substrate 16 of a first conductivity type (weakly n-doped) in which a semiconductor zone 33 of a second conductivity (p-doped) is disposed. This semiconductor zone 33 is located between transistor cells, which have p-doped base zones 34, 56 and n-doped source zones 40, 50, respectively. Gate electrodes 38, 46, 54, which are disposed above the semiconductor substrate, are insulated against the semiconductor body through insulating layers 37, 45, 53 (see column 8, line 12, lines 19-20, and line 44).

In contrast to the Examiner's opinion, no gate electrodes 38, 46, 54 can be connected to the semiconductor zone 33 of the second conductivity type due to the insulating layers. A contact 55, which contacts the semiconductor zone 33, is not connected to the gate potential V_{GATE} (see Fig. 3 and column 8, lines 46-47, the semiconductor zone 33 is connected to the cathode of the component by the contact 55).

Liao et al. also do not disclose such a component according to the invention of the instant application in which a semiconductor zone is doped complementarily to the

semiconductor substrate and is connected to a gate electrode of the component. As can be seen from Fig. 3 of Liao et al., the gate electrode 5 is completely insulated against the semiconductor body (with semiconductor zones 1, 2, 3, 6). Further, in Liao et al. there is also no semiconductor zone doped complementarily to the semiconductor substrate 1 in addition to the body zones 6 of the transistor cells.

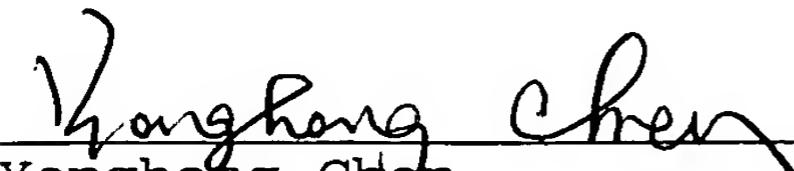
It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-4 and 6-19 are ultimately dependent on claim 1, they are believed to be patentable as well.

Finally, the Examiner has stated in the Advisory action dated November 22, 2004 that "even though there is insulation between the gate an[d] semiconductor zone it still is electrically connected." This argument is not understood. If there is an insulation layer 37 between the semiconductor zone 33 and the gate electrode 38, how could the semiconductor zone 33 be electrically connected to the gate electrode 38?

In view of the forgoing, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

Yonghong Chen
Reg. No. 56,150


Yonghong Chen

YC/bb

Date: January 24, 2005
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Claims Appendix:

Claim 1 (original): A vertical semiconductor component,
comprising:

a substrate of a first conductivity type having a first and a
second side;

an insulating layer covering said first side and having a
side remote from said substrate;

a more highly doped layer of the first conductivity type
applied on said second side;

a metallic drain contact applied on said more highly doped
layer;

a metallic gate contact;

a multiplicity of MOS cells on said first side of said
substrate for forming a first semiconductor switch, each MOS
cell having:

a first well of the second conductivity type, said first
well being introduced into said substrate and reaching
said first side;

a first metallic source contact extended through said insulating layer;

a first source region of the first conductivity type being incorporated into said well and having a potential, reaching to said first side of said substrate, and connecting to said first metallic source contact;

a first gate on said side of said insulating layer remote from said substrate, said first gate partly covering said well and connecting to said metallic gate contact;

a plurality of further MOS cells identical to said multiplicity of MOS cells, said further MOS cells having a second well , a second source region having a potential, a second gate on said first side of said substrate for forming a second semiconductor switch; and a second source contact electrically insulated from said first source contact and extending through said insulating layer; said second source regions of said further MOS cells connected to said second source contact on said first side; and

a region of the second conductivity type being incorporated into said substrate, reaching to said first side, and

electrically connecting to said second gate of said further MOS cells, said region having a potential floating relative to the potential of the first and second source regions of said MOS cells and further MOS cells.

Claim 2 (original): The vertical semiconductor component according to claim 1, wherein said region of the second conductivity type is surrounded exclusively by said further MOS cells, to form a structure for switching on said MOS cells.

Claim 3 (original): The vertical semiconductor component according to claim 2, wherein said switching-on structure is disposed adjacent said MOS cells of said first semiconductor switch.

Claim 4 (original): The vertical semiconductor component according to claim 2, wherein said switching-on structure is surrounded by said MOS cells.

Claim 6 (original): The vertical semiconductor component according to claim 2, including a lateral insulation provided between said MOS cells and said structure switching on said MOS cells.

Claim 7 (original): The vertical semiconductor component according to claim 1, wherein at least one of said further MOS cells is surrounded exclusively by regions of the second conductivity type, to form a structure for switching on said MOS cells.

Claim 8 (original): The vertical semiconductor component according to claim 7, wherein said switching-on structure is disposed adjacent said MOS cells of said first semiconductor switch.

Claim 9 (original): The vertical semiconductor component according to claim 7, wherein said switching-on structure is surrounded by said MOS cells.

Claim 10 (original): The vertical semiconductor component according to claim 7, including a lateral insulation provided between MOS cells and said structure switching on said MOS cells.

Claim 11 (original): The vertical semiconductor component according to claim 1, wherein:

said region is formed in the direction of said second side and holds a charge; and

a space charge zone is defined between said further MOS cells and said region, said space charge zone propagating the charge and driving said gate of the further MOS cells therewith.

Claim 12 (original): The vertical semiconductor component according to claim 11, wherein said region extends orthogonally from said first side toward said second side.

Claim 13 (original): The vertical semiconductor component according to claim 1, wherein said wells of said MOS cells and further MOS cells extend orthogonally from said first side to said second side.

Claim 14 (original): The vertical semiconductor component according to claim 1, including a plurality of said regions, some of said regions being laterally insulated from said further MOS cells and reaching into said substrate less than said wells of said MOS cells.

Claim 15 (original): The vertical semiconductor component according to claim 1, including a plurality of said regions, some of said regions being laterally insulated from said further MOS cells and doped to create a breakdown voltage less than a breakdown voltage of said MOS cells.

Claim 16 (original): The vertical semiconductor component according to claim 1, wherein the first conductivity type is n-conducting.

Claim 17 (original): The vertical semiconductor component according to claim 1, wherein said further MOS cells are connected in a cascaded manner.

Claim 18 (original): The vertical semiconductor component according to claim 1, wherein said regions are connected in a cascaded manner.

Claim 19 (original): The vertical semiconductor component according to claim 18, wherein said further MOS cells are also connected in a cascaded manner.